STMicroelectronics
ADG - ASD & IPAD™ Division[1]
BU Thyristors/Triacs

(1) ADG: Automotive and Discretes Group - ASD: Application Specific Device – IPAD™: Integrated Passive and Active Devices

PCN
Product/Process Change Notification

Wafer diameter production conversion to 150 mm

for DIACs products housed in DO-35 and MiniMelf packages

Notification number:	ADG-DIS/18/11095	**Issue Date**	20/09/2018
Issued by	Aline AUGIS		
Product series affected by the change		DB3xxx DB4xxx TMMDB3xxx **Specific devices** not expressly listed in the above table are included in this change.	
Type of change		Front end realization	

Description of the change

ST is converting to 150 mm wafers its DIACs housed in DO-35 and MiniMelf packages.
To align with current processes, their die metallization will be upgraded to Ti/Ag 6µm.

Reason for change

To pursue the standardization of its diffusion production lines, ST has qualified the 6-inch wafer diameter for its DIACs products.

This production upgrade is the result of the constant investments made by STMicroelectronics in the technology and the evolution of discrete devices. It illustrates the commitment of the Company to reinforce its leading position in the power discrete market.

Former versus changed product:	The changed products do not present modified electrical, dimensional or thermal parameters, leaving unchanged the current information published in the product datasheet The Moisture Sensitivity Level of the part (according to the IPC/JEDEC JSTD-020D standard) remains unchanged. The footprint recommended by ST remains the same. There is no change in the packing modes and the standard delivery quantities either. The products remain in full compliance with the ST ECOPACK®2 grade (“halogen-free”).

Disposition of former products

Delivery of the current product version will continue until the stock last.

Marking and traceability

The traceability of the devices diffused in 150mm wafers will be ensured by an internal codification and by the QA number.

Qualification complete date	September 2018

Forecasted sample availability

Product family	Commercial part number	Availability date
Diac	DB3	From week 41-2018
Diac	DB4	From week 41-2018

All other devices will be available 4 weeks after the request.

Change implementation schedule

Sales types	Estimated production start	Estimated first shipments
ALL	Week 41-2018	Week 51-2018

Comments:	

Customer's feedback

Please contact your local ST sales or quality representative contact for requests concerning this change notification.
Absence of acknowledgement of this PCN within 30 days of receipt will constitute acceptance of the change
Absence of additional response within 90 days of receipt of this PCN will constitute acceptance of the change

Qualification program and results	QRP18039 Attached

External Reliability Evaluation Report

Wafer diameter production conversion to 150 mm for DIACs products housed in DO-35 and MiniMelf packages

General Information		Locations	
Product Lines	*AC Switches*	**Wafer fab**	*ST Microelectronics Tours (FRANCE)*
Products Description	DB3 DB4 TMMDB3	**Assembly plant**	*Subcontractor 9954 (CHINA)*
Product Group	*ADG*	**Reliability Lab**	*STMicroelectronics Tours (FRANCE)*
Product division	*ASD & IPAD*	**Reliability assessment**	***PASS***
Package	*DO-35 and MiniMelf*		

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
Rev. 1	September 5th, 2018	10	Mickael ALCANTARA	Julien MICHELON	First issue

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD 22	Reliability test methods for packaged devices
JESD 47	Stress-Test-Driven Qualification of Integrated Circuits
JESD 94	Application specific qualification using knowledge based test methodology
MIL-STD-750C	Test method for semiconductor devices

2 GLOSSARY

BOM	Bill Of Materials
DUT	Device Under Test
HTRB	High Temperature Reverse Bias
P/N	Part Number
SS	Sample Size
TC	Temperature Cycling

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

Qualification of the wafer diameter production conversion to 150 mm for DIACs products housed in DO-35 and MiniMelf packages.

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the robustness of the products and safe operation, which is consequently expected during their lifetime.

Devices Characteristics

3.3 Devices description

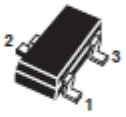
DB3 DB4 SMDB3

DIAC

FEATURES

- V_{BO} : 32V and 40V
- LOW BREAKOVER CURRENT

DO-35
(DB3 and DB4)



SOT-23
(SMDB3)*
Pin 1 and 3 must be shorted together

DESCRIPTION

Functioning as a trigger diode with a fixed voltage reference, the DB3/DB4 series can be used in conjunction with triacs for simplified gate control circuits or as a starting element in fluorenscent lamp ballasts.

A new surface mount version is now available in SOT-23 package, providing reduced space and compatibility with automatic pick and place equipment.

ABSOLUTE MAXIMUM RATINGS (limiting values)

Symbol	Parameter		Value	Unit
I_{TRM}	Repetitive peak on-state current tp = 20 µs F= 120 Hz	SMDB3	1.00	A
		DB3 / DB4	2.00	
Tstg Tj	Storage temperature range Operating junction temperature range		- 40 to + 125	°C

Note: * SMDB3 indicated as Preliminary spec as product is still in development stage.

October 2001 - Ed: 2B

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TMMDB3

DIAC

MINIMELF

FEATURES

- V_{BO} : 32V
- Breakover voltage range: 28 to 36V

DESCRIPTION

Functioning as a trigger diode with a fixed voltage reference, the TMMDB3 can be used in conjunction with triacs for simplified gate control circuits or as a starting element in fluorescent lamp ballasts.

ABSOLUTE MAXIMUM RATINGS (limiting values)

Symbol	Parameter	Value	Unit
I_{TRM}	Repetitive peak on-state current tp = 20 µs F= 120 Hz	2	A
Tstg Tj	Storage temperature range Operating junction temperature range	- 40 to + 125	°C

4 TESTS RESULTS SUMMARY

4.1 Test vehicles

Two test vehicles were chosen:

- **DB3**
- **DB4**

Lot #	Part number	Package	Comment
Lot 1	DB3	DO-35	Qualification lot 1
Lot 2	DB4	DO-35	Qualification lot 2
Lot 3	DB3	DO-35	Qualification lot 3
Lot 4	DB4	DO-35	Qualification lot 4

4.2 Test plan and results summary

Test	Std ref.	Conditions	SS	Steps	Failure/SS			
					Lot 1	Lot 2	Lot 3	Lot 4
HTRB	JESD22 A-108 MIL-STD-750C method 1040	T_j = 125 °C 28V VAC (DB3) or 32V VAC (DB4)	231	168 h	**0/77**	**0/77**	**0/77**	
				500 h	**0/77**	**0/77**	**0/77**	
				1000 h	**0/77**	**0/77**	**0/77**	
TC	JESD22 A-104	-65 °C/+150 °C 2 cycles/h	231	500 cycles		**0/77**	**0/77**	**0/77**

5 ANNEXES

5.1 Device details

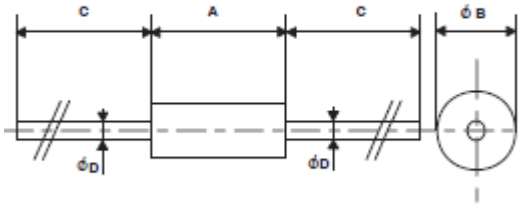
5.1.1 Pin connection

DO-35
(DB3 and DB4)

MINIMELF

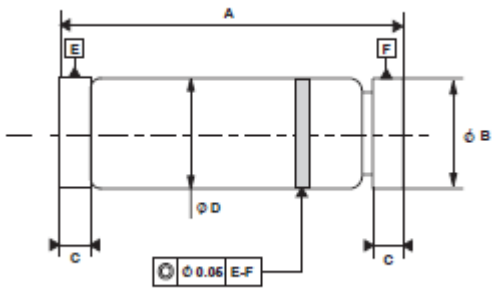
5.1.2 Package outline/Mechanical data

DO-35 package



REF.	DIMENSIONS			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	3.05	4.50	0.120	0.177
B	1.53	2.00	0.060	0.079
C	28.00		1.102	
D	0.458	0.558	0.018	0.022

MINIMELF package



REF.	DIMENSIONS					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	3.30	3.40	3.6	0.130	0.134	0.142
B	1.59	1.60	1.62	0.063	0.063	0.064
C	0.40	0.45	0.50	0.016	0.018	0.020
D		1.50			0.059	

5.2 Tests Description

Test name	Description	Purpose
Die-oriented test		
HTRB (AC mode) High Temperature Reverse Bias	The device is stressed here in DC mode, trying to satisfy as much as possible the following conditions: - Low power dissipation. - Peak supply voltage compatible with diffusion process and internal circuitry limitations.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide aging, layout sensitivity to surface effects.
Die and Package-oriented test		
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.